11-20-00 A

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: VTI1P304A

First Named Inventor: Rao V. Annapragada

UTILITY PATENT APPLICATION TRANSMITTAL (37 CFR. § 1.53(b))

(Continuation, Divisional or Continuation-in-part application)

Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

☐ Duplicate for fee processing

Sir: This is a request for filing a patent application under 37 CFR. § 1.53(b) in the name of inventor:
Rao V. Annapragada

For: METHODS FOR MAKING RELIABLE VIA STRUCTURES HAVING HYDROPHOBIC INNER WALL SURFACES

This application is a ☐ Continuation ☒ Divisional ☐ Continuation-in-part of prior Application No.: **09/234,235**, from which priority under 35 U.S.C. §120 is claimed.

Application Elements:

- ☒ 20 Pages of Specification, Claims and Abstract
- ☒ 10 Sheets of **formal** Drawings
- ☒ 02 Declaration
  - ☐ Newly executed (original or copy)
  - ☒ Copy from a prior application (37 CFR 1.63(d) for a continuation or divisional). The entire disclosure of the prior application from which a copy of the declaration is herein supplied is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
    - ☐ Deletion of inventors Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

Accompanying Application Parts:

- ☐ Assignment and Assignment Recordation Cover Sheet (recording fee of $40.00 enclosed)
- ☐ Power of Attorney
- ☐ 37 CFR 3.73(b) Statement by Assignee
- ☐ Information Disclosure Statement with Form PTO-1449 ☐ Copies of IDS Citations

☒ Preliminary Amendment (*New claims numbered after highest original claim in prior application.*)

☒ Return Receipt Postcard

☐ Small Entity Statement(s) ☐ Statement filed in prior application. Status still proper and desired.

☐ Other:

Claim For Foreign Priority

☐ Priority of _____ Application No. _____ filed on _____ is claimed under 35 U.S.C. § 119.

☐ The certified copy has been filed in prior application U.S. Application No. _____

☐ The certified copy will follow.

Extension of Time for Prior Pending Application

☐ A Petition for Extension of Time is being concurrently filed in the prior pending application. A copy of the Petition for Extension of Time is attached.

Amendments

☒ Amend the specification by inserting before the first line the sentence: "This is a

☐ Continuation ☐ Continuation-in-part ☒ Divisional application of copending prior

☒ Application No. 09/234,235 filed on January 20, 1999,

☐ International Application _____ filed on _____ which designated the United States,

the disclosure of which is incorporated herein by reference."

☒ Cancel in this application original claims 1-20 of the prior application before calculating the filing fee. (*At least one original independent claim must be retained.*)

Fee Calculation (37 CFR § 1.16)

	(Col. 1) NO. FILED	(Col. 2) NO. EXTRA	SMALL ENTITY RATE	FEE	OR	LARGE ENTITY RATE	FEE
BASIC FEE			$355	$	OR	$710	$710.00
TOTAL CLAIMS	15 -20 =	00	x09 =	$	OR	x18 =	$
INDEP CLAIMS	03 -03 =	00	x40 =	$	OR	x80 =	$
[ ] Multiple Dependent Claim Presented			$135 =	$	OR	$270 =	$
* If the difference in Col. 1 is less than zero, enter "0" in Col. 2.			Total	$	OR	Total	**$710.00**

☒ Check No. 4490 in the amount of $710.00 is enclosed.

☒ The Commissioner is authorized to charge any fees beyond the amount enclosed which may be required, or to credit any overpayment, to Deposit Account No. 50-0805 (Order No. VTI1P304A).

General Authorization for Petition for Extension of Time (37 CFR §1.136)

☒ Applicants hereby make and generally authorize any Petitions for Extensions of Time as may be needed for any subsequent filings. The Commissioner is also authorized to charge any extension fees under 37 CFR §1.17 as may be needed to Deposit Account No. 50-0805 (Order No. VTI1P304A).

☒ Please send correspondence to the following address:

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Date: November 16, 2000

Albert S. Penilla, Esq.
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	) Docket No: VTI1P304A
R. Annapragada	) Group Art Unit: 2813
Application No: Unknown	) Examiner: Unknown
Filed: November 16, 2000	) November 16, 2000
For: RELIABLE VIA STRUCTURES HAVING HYDROPHOBIC INNER WALL SURFACES (as amended)	)

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail to: Commissioner of Patents and Trademarks, Washington, DC 20231 on November 16, 2000.

Signed: Kay Harlow
Kay Harlow

AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Please enter the following preliminary amendments and remarks:

IN THE TITLE

Please amend the title as follows.

Please change the title to --RELIABLE VIA STRUCTURES HAVING HYDROPHOBIC INNER WALL SURFACES--.

IN THE CLAIMS

Please amend the claims as follows. All pending claims after this amendment are listed below for the convenience of the Examiner. Claims amended by the Amendment are indicated as such.

21. A semiconductor via structure being defined through an inter-metal dielectric, comprising:

a first conductive pattern element; and

a layer of SOG material formed over the first conductive pattern element, the layer of SOG material having a via hole defined therethrough, such that the via hole defines a path to the first conductive pattern element,

wherein the via hole has a via wall surface, the via wall surface is defined along the SOG material that extends to the first conductive pattern element, and the via wall surface has a hydrophobic material layer.

22. A semiconductor via structure being defined through an inter-metal dielectric as recited in claim 21, wherein the hydrophobic material layer is a reaction product of silicon dioxide and a halogen compound.

23. A semiconductor via structure being defined through an inter-metal dielectric as recited in claim 22, wherein the halogen compound is NH_4F.

24. A semiconductor via structure being defined through an inter-metal dielectric as recited in claim 22, wherein the halogen compound is CCl_4.

25. A semiconductor via structure being defined through an inter-metal dielectric as recited in claim 23, further comprising:

a layer coating the via hole in direct substantially continuous contact with the hydrophobic material layer, the layer coating being a titanium nitride material.

26. A semiconductor via structure being defined through an inter-metal dielectric as recited in claim 25, further comprising:

a conductive fill material contained within the via hole and in direct substantially continuous contact with the layer coating.

27. A semiconductor via structure being defined through an inter-metal dielectric as recited in claim 26, further comprising:

a second conductive pattern element in conductive contact with the conductive fill material, the titanium nitride material, and the first conductive pattern element, thereby defining a reliable conductive interconnection between a first metal layer network that includes the first conductive pattern element and a second metal layer network that includes the second conductive pattern element.

Please add the following new claims:

28. (New) A semiconductor via structure, comprising:

a first conductive pattern element; and

a layer of spin-on-glass material formed over the first conductive pattern element, the layer of spin-on-glass material having a via hole defined therethrough,

such that the via hole defines a path to the first conductive pattern element, wherein the via hole has a via wall surface, the via wall surface is defined along the spin-on-glass material that extends to the first conductive pattern element, and the via wall surface has a hydrophobic material layer that is a reaction product of silicon dioxide and a halogen compound.

29. (New) A semiconductor via structure as recited in claim 28, wherein the halogen compound is NH_4F.

30. (New) A semiconductor via structure as recited in claim 28, wherein the halogen compound is CCl_4.

31. (New) A semiconductor via structure as recited in claim 29, further comprising:

a layer coating the via hole in direct substantially continuous contact with the hydrophobic material layer, the layer coating being a titanium nitride material.

32. (New) A semiconductor via structure as recited in claim 31, further comprising:

a conductive fill material contained within the via hole and in direct substantially continuous contact with the layer coating.

33. (New) A semiconductor via structure, comprising:

a substrate; and

a layer of spin-on-glass material formed over the substrate, the layer of spin-on-glass material having a via hole defined therethrough, such that the via hole defines a path to the substrate, wherein the via hole has a via wall surface, the via wall surface is defined along the spin-on-glass material that extends to the substrate, and the via wall surface has a hydrophobic material layer that is a reaction product of silicon dioxide and a halogen compound, the halogen compound being selected from one of NH_4F and CCl_4; and

a layer coating the via hole in direct substantially continuous contact with the hydrophobic material layer.

34. (New) A semiconductor via structure as recited in claim 33, wherein the layer coating is a titanium nitride material.

35. (New) A semiconductor via structure as recited in claim 34, further comprising:

a conductive fill material contained within the via hole and in direct substantially continuous contact with the layer coating.

REMARKS

The Applicants respectfully request that new claims 28-35 be entered before the examination of the present application. Claims 1-20 have been canceled.

The Applicants respectfully submit that all of the pending claims are in condition for allowance. A notice of allowance is respectfully requested. If the Examiner has any questions concerning the present amendment, the Examiner is kindly requested to contact the undersigned at (408) 749-6903. If any additional fees are due in connection with filing this amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. VTI1P304A). A duplicate copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
MARTINE PENILLA & KIM, L.L.P.

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ATTORNEY DOCKET No.
VTI1P204

PATENT APPLICATION

RELIABLE VIA STRUCTURES HAVING HYDROPHOBIC INNER WALL SURFACES AND METHODS FOR MAKING THE SAME

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RELIABLE VIA STRUCTURES HAVING HYDROPHOBIC INNER WALL SURFACES AND METHODS FOR MAKING THE SAME

by Inventor

Rao V. Annapragada

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to reliable semiconductor via structures, and more particularly, the present invention relates to techniques for converting silicon dioxide layer regions within via hole walls into moisture repellant hydrophobic layer regions.

2. Description of the Related Art

In the fabrication of semiconductor devices, various layers are provided with conductive material, such as metal lines. The metal lines are commonly formed over successive insulating dielectric layers. Accordingly, it is generally necessary to electrically interconnect the metal lines between the dielectric layers. To accomplish this, vias (or via holes) are formed through the dielectric layers to electrically interconnect selected metal lines or features.

Spin on glass material ("SOG material") is used for some of the dielectric layers. For example, so-called "true" SOG materials, such as that sold under the brand name "LSU 418," which is available from Allied Signal, Inc. of Sunnyvale, California, is used because it has a low k characteristic (e.g., dielectric constant less than 4.0, which is common for silicon dioxide). Many "SOG-like" materials also have a low k characteristic. The SOG-like materials may, for example, be spin coated or result from vapor deposition using methyl silane and hydrogen peroxide chemistry. However, both the true SOG materials and the SOG-like materials oxidize during and after an operation

known as ashing. Ashing is commonly performed to remove a photoresist layer that has been spin coated over the SOG material to facilitate patterning operations. Unfortunately, the oxidized SOG materials are known to absorb too much moisture from the atmosphere, in that during later operations (such as, for example, during metal deposition), the absorbed moisture outgasses causing poisoning of the vias. Such poisoning prevents adequate electrical connections from being made, *e.g.*, between the opposite metal layers which are to be interconnected by way of the conductive material in the vias.

Unfortunately, prior art attempts to reduce the amount of the moisture retained by the oxidized SOG materials have not been successful. For example, if thermal outgassing is performed at a high enough temperatures to remove adequate amounts of the moisture (e.g., at about 700 degrees C) from the oxidized SOG materials, significant problems result. These high outgassing temperatures are generally considered too excessive for the metal layers to withstand without causing damage (*e.g.*, metal layers of aluminum may deform). Also, the SOG material is not stable at the high outgassing temperatures. If lower temperatures are used in an attempt to reduce the moisture retained by the oxidized SOG materials (*e.g.*, at 400 to 450 degrees C in a PVD chamber), although the metal lines may not be damaged by the temperature, not enough of the moisture is removed. The remaining moisture then outgasses during later attempts to deposit via coating/filling materials such as titanium nitride (TiN) and tungsten (W) metal layers (which are commonly used for the conductive vias), and such outgassing prevents proper continuous deposition of these metal layers in the internal via walls. For example, the outgassing moisture may prevent tungsten from being deposited

on the walls of the via, and the TiN will tend to deposit discontinuously (*e.g.*, in separate random groups), rather than in a complete conductive layer.

To facilitate this discussion, Figure 1A shows a semiconductor structure including a substrate 101 supporting a first conductor 102, such as a metal line, which is to be in contact with a second conductor 103, such as a conductive layer of titanium nitride shown in Figure 1C. Deposited on the substrate 101 is a layer 104 of SOG material, which may include both true SOG materials, materials having a SOG-like characteristic, and other organic low-K dielectric materials. Accordingly, such characteristic includes having a low dielectric constant (K), and oxidizing during photoresist ashing to form a surface layer 106 of silicon dioxide. After deposition of a silicon dioxide layer 107 on the layer 104 of SOG material, a via hole 109 is formed through the silicon dioxide layer 107 and through the SOG material layer 104 to expose the metal 102 as shown in Figure 1A.

Between the etching operation and a subsequent deposition operation, a semiconductor structure 111 defined by the substrate 101 and the layers 102, 104, and 107, is exposed to oxygen in the atmosphere. The oxygen thus causes the inner wall surface of the via hole 109 to oxidize and form the surface layer 106. As described above, the surface layer 106 is very porous, is prone to collect moisture, and upon being heated, releases gaseous moisture.

The effect of the release of the moisture is shown in Figure 1C, which depicts operations intended to deposit a layer 103 of titanium nitride under a layer 114 of tungsten. The purpose of the titanium nitride layer 103 is to electrically interconnect the first conductor 102 to the tungsten layer 114. However, Figure 1C shows arrows 116 depicting moisture being outgassed from the surface layer 106 during the deposition of the titanium nitride layer 103. The outgassed moisture prevents the layer 103 of titanium

nitride from being continuous, as illustrated by the spaced pieces 103a of titanium nitride. It may be understood, then, that the word "layer" in the phrase "layer 103" denotes the desired form of the titanium nitride, whereas the actual form of the prior art titanium nitride layer is discontinuous as shown in Figure 1C. Because the pieces 103a are spaced, the desired electrical interconnection from the metal 102 to the tungsten 114 is not achieved.

Moreover, when an attempt is made to deposit the tungsten layer 114 after the titanium nitride pieces 103a, the tungsten layer 114 tends to stop short of filling the via, leaving a void 119 shown in Figures 1C and 1D. The void 119 is filled with neither titanium nitride nor tungsten, such that there is a high likelihood that there will be no electrical conductivity from the metal 102 to the tungsten layer 114.

In view of the forgoing, there is an unfilled need for a reliable semiconductor via structure, and a method of making reliable via structures to prevent outgassing problems and associated via hole voids.

SUMMARY OF THE INVENTION

Broadly speaking, the present invention fills these needs by providing improved semiconductor device via structures having an inner hydrophobic wall surface layer to prevent the aforementioned moisture absorption and subsequent outgassing. Such via structures are made using techniques for converting a silicon dioxide inner wall layer into the desirable hydrophobic layer, thus preventing the failure inducing voids in the via structures. It should be appreciated that the present invention can be implemented in numerous ways, including as a process, an apparatus, a system, a device, or a method. Several inventive embodiments of the present invention are described below.

In one embodiment, a method of making a via hole in a semiconductor structure is disclosed. The via hole has a surface layer of hydrophobic material, and includes an outer layer of a material having a characteristic of SOG materials. The characteristic is that the outer layer oxidizes during photoresist ashing to form a surface layer of silicon dioxide in the via hole. In the method, an operation is performed after the ashing. The operation includes performing a chemical dehydroxylation operation on the surface layer of silicon dioxide to convert the surface layer of silicon dioxide to the surface layer of hydrophobic material. To achieve this, the semiconductor structure is placed in a closed process chamber, and then, a halogen compound is admitted into the process chamber to facilitate the chemical dehydroxylation operation. In this embodiment, the halogen compound is selected from either NH_4F, other gaseous combination including fluorine, or CCl_4.

In an other embodiment, a method of making a via hole in a semiconductor device is disclosed. The method includes defining a via hole having a wall surface that at least partially has a characteristic of spin on glass materials. The characteristic being that the wall surface oxidizes during a photoresist ashing operation and the oxidizing converts the

wall surface into a silicon dioxide skin. The method then includes placing the semiconductor device in a process chamber. Once the semiconductor device is placed in the process chamber, the method includes introducing a halogen gas into the process chamber to cause a chemical dehydroxylation of the silicon dioxide skin to thereby convert the silicon dioxide skin into a hydrophobic material skin, such that the hydrophobic skin is part of the wall surface of the via hole.

In still another embodiment, a semiconductor via structure that is configured to be defined through an inter-metal dielectric is disclosed. The structure includes a first conductive pattern element. A layer of SOG material formed over the first conductive pattern element. The layer of SOG material having a via hole defined therethrough, such that the via hole defines a path to the first conductive pattern element. The via hole has a via wall surface that is defined along the SOG material that extends to the first conductive pattern element, and the via wall surface has a hydrophobic material layer. In this embodiment, the hydrophobic material layer is a reaction product of silicon dioxide and a halogen compound. The halogen compound may be NH_4F or CCl_4, and when the CCl_4 is used, the via hole fill material that will be in contact with the hydrophobic material layer is preferably copper.

As an advantage of each of such embodiments, no high temperature outgassing is required to avoid the disadvantages of the oxidized SOG layer, *e.g.*, the silicon dioxide layer that is formed in the SOG after typical ashing operations. Other aspects and advantages of the present invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be readily understood by the following detailed description in conjunction with the accompanying drawings. Therefore, like reference numerals designate like structural elements.

Figure 1A is a cross sectional view of a prior art semiconductor structure showing a via formed through a layer of SOG material at a location defined by photoresist;

Figure 1B is a cross sectional view of the semiconductor structure shown in Figure 1A after an ashing operation has been performed to remove the photoresist, wherein an undesired surface layer of oxidized SOG material is formed after the ashing operation;

Figure 1C is a cross sectional view of the semiconductor structure shown in Figures 1A and 1B after an unsuccessful attempt to deposit a complete layer of titanium nitride, showing an undesired discontinuous characteristic of the titanium nitride caused by outgassing of the undesired surface layer of oxidized SOG material;

Figure 1D is an enlarged view of a portion of the structure shown in Figure 1C, illustrating a void defined due to the failure of a tungsten layer to be deposited completely in the via hole surface walls due to outgassing of moisture from the undesired surface layer of oxidized SOG material;

Figure 2A is a cross sectional view of the semiconductor structure shown in Figure 1B, showing a process of the present invention including a chemical dehydroxylation operation performed on the surface layer of silicon dioxide to convert

the surface layer of silicon dioxide to provide the surface layer of hydrophobic material of the present invention;

Figure 2B is a schematic view of a process chamber in which the chemical dehydroxylation operation is performed, showing the semiconductor structure with the surface layer of silicon dioxide which is to be converted to the surface layer of hydrophobic material of the present invention;

Figure 2C is a schematic illustration of the process of converting the silicon dioxide layer to the hydrophobic layer;

Figure 2D is a cross sectional view of the semiconductor structure shown in Figure 2A, showing a result of the process of the present invention as including the provision of the surface layer of hydrophobic material of the present invention;

Figure 3A is a flow chart depicting operations of the process of the present invention; and

Figure 3B is a flow chart illustrating sub-operations of a chemical dehydroxylation operation shown in Figure 3A.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

An invention for reliable via structures, and methods for making reliable via structures in semiconductor devices, which circumvent the aforementioned problems of via voids and associated outgassing, is disclosed. In a preferred embodiment, the reliable via structures are made to have a via wall surface layer that is hydrophobic. As such, the via wall surface layer will substantially not absorb moisture, which is a major contributing factor of conductive via voids. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be understood, however, to one skilled in the art, that the present invention may be practiced without some or all of these specific details. In other instances, well known process operations have not been described in detail in order not to obscure the present invention.

Figure 2A shows one embodiment of a chemical dehydroxylation operation of the present invention performed on the surface layer 106 of silicon dioxide to convert such layer 106 to a hydrophobic material. The operation may be performed on SOG material of the layer 104, such material having the characteristic of spin on glass. The SOG material is taken from the group consisting of the true spin on glass described above, and the SOG-like material described above as including, for example, an organic vapor-deposited low thermal expansion coefficient material, and other spin coated low K dielectrics. Such SOG material of the layer 104 has the characteristic of spin on glass as shown in Figure 1C, and has the oxidized surface layer 106 of silicon dioxide. The chemical dehydroxylation operation uses a halogen compound.

Figure 2B shows an example chamber apparatus for performing the chemical dehydroxylation operation in accordance with this embodiment. The chemical dehydroxylation operation is performed by placing the semiconductor structure of Figure 2A in a closed process chamber 122. It should be noted that many types of chambers may be used, and one or more wafers may be placed in a chamber at one time. For example, when more than one wafer is placed in the chamber in a batch, the wafers are preferably held in a wafer carrier. A halogen supply 123 is configured to be admitted into the closed process chamber 122, such that the halogen compound is capable of facilitating the chemical dehydroxylation operation. The preferred flow rate of the halogen supply is preferably set between about 10 sccm and about 50 sccm, and most preferably set to about 20 sccm. The halogen compound used in the chemical dehydroxylation operation may be NH_4F or CCl_4, for example. Upon causing the chemical dehydroxylation operation, by-product gases, such as, NH_3 and vapor H_2O are believed to be formed. These by-product gases may then be removed from the chamber using any number of conventional techniques.

Figure 2C schematically shows the reaction of surface OH groups (*i.e.*, Si-OH) of the silicon dioxide of surface layer 106 with the NH_4F. The silicon dioxide of the layer 106 is shown reacting with the NH_4F, such that the fluorine (F) vapors replace the OH groups, and thereby results in a hydrophobic layer 121. The hydrophobic layer is thus Si_sF. Of course, other fluorine containing gases may also be used to cause the replacement of the OH groups and produce the hydrophobic layer 121.

Figure 2D schematically depicts the result of the chemical dehydroxylation operation, illustrating the hydrophobic layer 121 as a layer that defines the walls of the via hole. The hydrophobic layer 121 is shown having the fluorine (F) at the surface,

instead of the porous OH interface shown at the surface of the layer 106 in Figure 2A. Significantly, Figure 2D shows the titanium nitride layer 103 as being a continuous layer which is permitted to be deposited in such continuous manner against the surface of the hydrophobic layer 121. Further, Figure 2D shows the tungsten layer 114 filling the via hole substantially against the continuous surface of layer 103, and thereby making a good electrical contact with the first conductor 102.

A process of the present invention may include a series of operations depicted in Figure 3A. The process may start with a structure such as that shown in prior Figure 1A, where an operation 132 spin coats the photoresist layer 108 onto the silicon dioxide layer 107 to define the intended location and size of a via, or a plurality of vias of an integrated circuit device. An operation 134 then etches the via hole or holes in the layers 104 and 107. An ashing operation 136 is performed to remove the photoresist and define the structure shown in Figure 1B, and the SOG layer 104 is exposed in operation 137 to atmosphere and becomes oxidized. As a result, the surface layer 106 becomes defined in the SOG layer 104 as shown in Figure 1B. Further processing is performed in an operation 138 to remove side wall polymers (not shown) formed during etching, for example. Such removal is typically done using a wet solvent stripper.

To avoid the disadvantages of the prior art, the process of the present invention includes a chemical dehydroxylation operation 142, as described above. In more detail, this operation 142 includes sub-operations shown in Figure 4B, including an admitting sub-operation 144 by which the halogen compound is introduced into a closed process chamber 122. The admitting operation 144 is performed until the pressure in the chamber 122 is broadly from about 1.5 to 3.0 atmospheres, and is more preferably from about 1.5 and about 2.0 atmospheres. In a sub-operation 146, the temperature in the chamber 122 is

controlled to be from about 100 degrees C to less than about 450 degrees C, and more preferably from about 100 degrees C to less than about 200 degrees C, and most preferably at about 120 degrees C. In an operation 148, the chemical dehydroxylation operation 142 is performed for a period from about 0.5 to 6 minutes, and more preferably for a period of about 1 minutes to about 3 minutes, and most preferably for 2 minutes. The operation 142, including the sub-operations 144, 146, and 148, results in the forming of the hydrophobic layer 121 shown in Figure 2D, which is the surface of the via hole onto which it is desired to deposit the titanium nitride layer 103.

When the halogen compound used in the operation 142 is NH_4F, a physical vapor deposition (PVD) operation 152 may be used to deposit the continuous titanium nitride layer 103 in the via hole or via holes, which results in a continuous, conductive layer being provided over and in contact with the hydrophobic layer 121 and in electrical contact with the first conductor 102. In Figure 2D, such continuous layer 103 is distinguished from the discontinuous layer 103/103a shown in Figures 1C and 1D.

Then, in an operation 154, a chemical vapor deposition (CVD) operation may be used to deposit the tungsten layer 114 in the via hole and in direct contact with the titanium nitride layer 103. The tungsten layer 114 is also a continuous layer, that is, a layer that completely fills the via hole and that is in direct electrical contact with substantially all of the titanium nitride layer 103. Then, a chemical mechanical polishing (CMP) operation is used to planarize the top of the via hole of Figure 2D. For example, the CMP operation will preferably remove the excess tungsten material and TiN material down to the layer 107. Following the CMP operation, an operation 158 determines whether there are any more semiconductor structures, *i.e.*, conductive vias to fabricate at other layers of the semiconductor device. If the determination is yes, then a loop 160 is

taken to operation 132, and such operation 132 is performed for the next via structure or structures. If the determination is no, then after the operation 158, the operations ends.

A further embodiment of the present invention contemplates the halogen compound being CCl_4, rather than NH_4F in the chemical dehydroxylation operation 142, and more specifically in the admitting operation 144. In this embodiment, in the operation 152, copper is preferably used to fill the via holes over the surface layer 121 of hydrophobic material. After the copper layer, further operations may be performed as described above, resuming with operation 156.

It should be understood then, that an advantage of each of the described embodiments is that no high temperature outgassing is required to avoid the disadvantages of the porous surface layer 106 of silicon dioxide. Instead of such undesired high temperature outgassing, the layer 106 is converted into the hydrophobic layer 121, which thus allows the titanium nitride materials, copper materials, aluminum materials, or any other type of via fill metallization to be properly deposited in the via hole. Thus, the resulting via hole structures will be substantially more reliable than conventional via structures.

Although the foregoing invention has been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the invention is not to be limited to the details given herein, but may be modified within the scope and equivalents of the appended claims.

What is claimed is:

Claims

1. A method of making a via hole in a semiconductor structure, the via hole having a surface layer of hydrophobic material, the via hole comprising an outer layer of material having a characteristic of spin on glass materials, the characteristic being that the outer layer oxidizes during photoresist ashing to form a surface layer of silicon dioxide in the via hole; the method comprising the operation of:

performing a chemical dehydroxylation operation after the ashing on the surface layer of silicon dioxide to convert the surface layer of silicon dioxide to the surface layer of hydrophobic material.

2. The method of claim 1, wherein the material of the outer layer having the characteristic of spin on glass is taken from the group consisting of spin on glass and an organic vapor-deposited low thermal expansion coefficient material.

3. The method of claim 1, wherein the performing of the operation of chemical dehydroxylation is by the operations of:

placing the semiconductor structure in a closed process chamber, the semiconductor structure having the via hole with the surface layer of silicon dioxide; and

admitting into the process chamber a halogen compound configured to facilitate for the chemical dehydroxylation operation.

4. The method of claim 3, further comprising:

performing the admitting operation until the pressure in the chamber is from about 1.5 to about 3 atmospheres;

maintaining a temperature in the chamber from about 100 degrees C to less than about 450 degrees C; and

performing the admitting and maintaining operations for a period ranging between about 1 minute and about 4 minutes.

5. The method according to claim 1, wherein the chemical dehydroxylation operation produces by-products, and further comprising:

removing the by-products from the chamber.

6. The method according to claim 3, wherein the halogen compound is NH_4F.

7. The method according to claim 3, wherein the halogen compound is CCl_4

8. The method according to claim 7, further comprising:

depositing a layer of titanium nitride (TiN) in the via hole over the surface layer of hydrophobic material.

9. The method according to claim 3, further comprising:

pressurizing the chamber with the halogen compound from about 1.5 to about 3 atmospheres.

10. The method according to claim 9, wherein the pressurizing is at a pressure of about 2.0 atmospheres.

11. The method according to claim 3, wherein the operation of admitting the halogen compound into the process chamber is performed at a rate ranging between about 10 sccm and about 50 sccm.

12. The method according to claim 3, wherein the operation of admitting the halogen compound into the process chamber is performed at a temperature of about 100 degrees C to about 300 degrees C.

13. The method according to claim 2, wherein the material of the **outer** layer is spin on glass and the chemical dehydroxylation operation is performed on the surface layer of silicon dioxide using NH_4F to convert the surface layer of silicon dioxide to the hydrophobic material.

14. The method according to claim 13, further comprising:

performing the chemical dehydroxylation operation for a period of about 2 minutes.

15. A method of making a via hole in a semiconductor device, the method comprising;

defining a via hole having a wall surface that at least partially has a characteristic of spin on glass materials, the characteristic being that the wall surface oxidizes during a photoresist ashing operation and the oxidizing converts the wall surface into a silicon dioxide skin;

placing the semiconductor device in a process chamber; and

introducing a halogen gas into the process chamber to cause a chemical dehydroxylation of silicon dioxide skin to thereby convert the silicon dioxide skin into a hydrophobic material skin, the hydrophobic skin being part of the wall surface of the via hole.

16. The method of claim 15, wherein the halogen gas is selected from one of an NH_4F gas and a $CC1_4$ gas.

17. The method according to claim 15, wherein the process chamber is maintained at a pressure ranging between about 1.5 and about 3 atmospheres.

18. The method of claim 16, wherein the hydrophobic material skin is one of an Si_sF and a $CC1_4F$.

19. The method of claim 16, further comprising:

maintaining a temperature of the process chamber from about 100 degrees C to less than about 450 degrees C.

20. The method of claim 16, wherein the converting is performed during a time period ranging between about one minute and about four minutes.

21. A semiconductor via structure being defined through an inter-metal dielectric, comprising:

a first conductive pattern element; and

a layer of SOG material formed over the first conductive pattern element, the layer of SOG material having a via hole defined therethrough, such that the via hole defines a path to the first conductive pattern element,

wherein the via hole has a via wall surface, the via wall surface is defined along the SOG material that extends to the first conductive pattern element, and the via wall surface has a hydrophobic material layer.

22. A semiconductor via structure being defined through an inter-metal dielectric as recited in claim 21, wherein the hydrophobic material layer is a reaction product of silicon dioxide and a halogen compound.

23. A semiconductor via structure being defined through an inter-metal dielectric as recited in claim 22, wherein the halogen compound is NH_4F.

24. A semiconductor via structure being defined through an inter-metal dielectric as recited in claim 22, wherein the halogen compound is CCl_4.

25. A semiconductor via structure being defined through an inter-metal dielectric as recited in claim 23, further comprising:

a layer coating the via hole in direct substantially continuous contact with the hydrophobic material layer, the layer coating being a titanium nitride material.

26. A semiconductor via structure being defined through an inter-metal dielectric as recited in claim 25, further comprising:

a conductive fill material contained within the via hole and in direct substantially continuous contact with the layer coating.

27. A semiconductor via structure being defined through an inter-metal dielectric as recited in claim 26, further comprising:

a second conductive pattern element in conductive contact with the conductive fill material, the titanium nitride material, and the first conductive pattern element, thereby defining a reliable conductive interconnection between a first metal layer network that includes the first conductive pattern element and a second metal layer network that includes the second conductive pattern element.

RELIABLE VIA STRUCTURES HAVING HYDROPHOBIC INNER WALL SURFACES AND METHODS FOR MAKING THE SAME

ABSTRACT OF THE DISCLOSURE

Disclosed is a method of making a reliable via hole in a semiconductor device layer, and a reliable via structure having internal wall surface layers that are hydrophobic, and thereby are non-moisture absorbing. The inner wall of the via structure has a layer of material having a characteristic of spin on glass (SOG), such that the characteristic is that the outer layer of the SOG oxidizes during photoresist ashing to form a surface layer of silicon dioxide in the via hole wall. In the method, the via structure is placed through a chemical dehydroxylation operation after the ashing operation, such that the layer of silicon dioxide in the via hole wall is converted into a hydrophobic material layer. The conversion is performed by introducing a halogen compound suitable for the chemical dehydroxylation operation, wherein the halogen compound may be NH_4F or CCl_4.

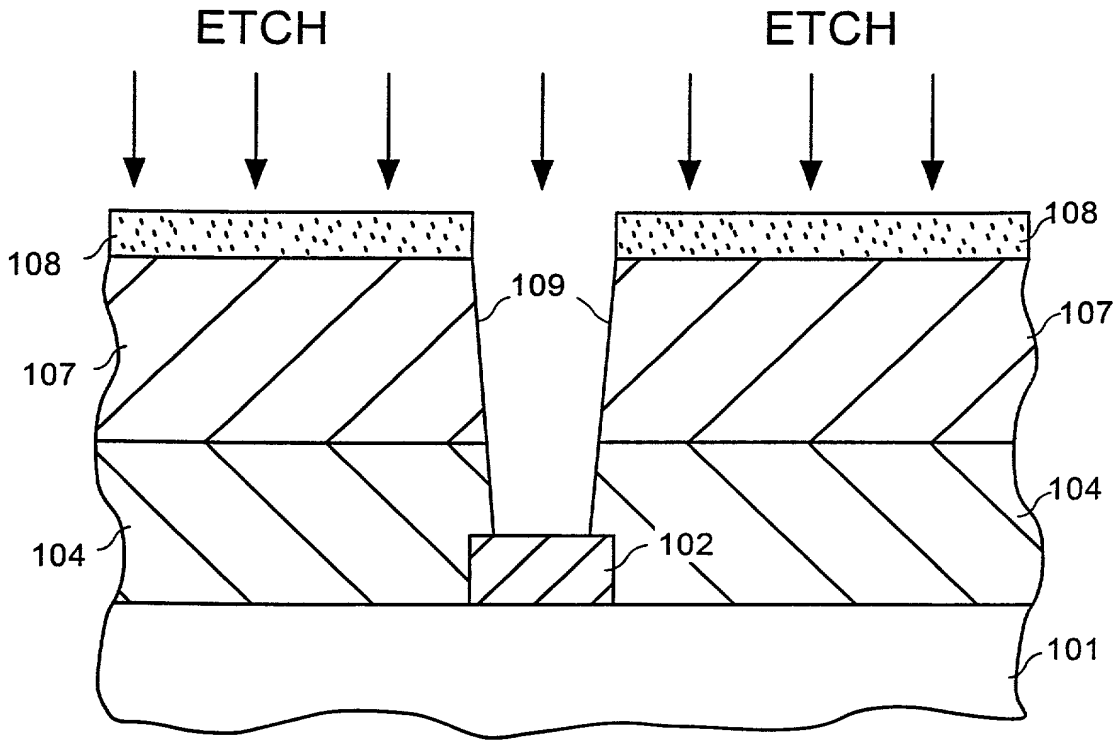

FIG. 1A
(prior art)

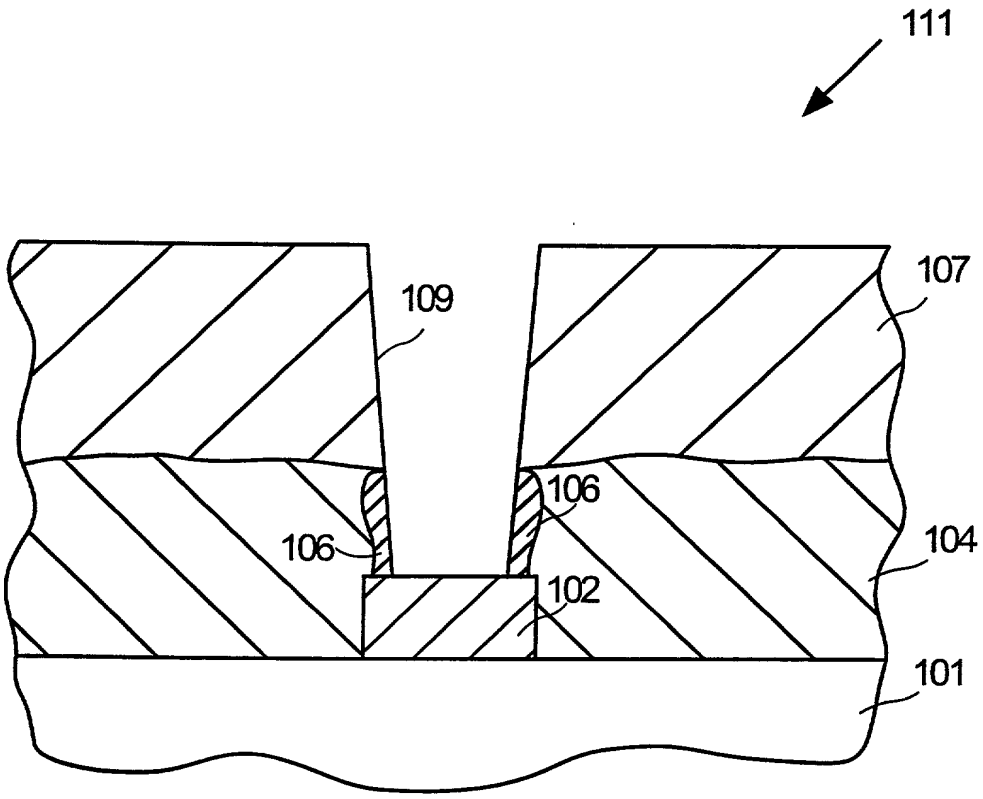

FIG. 1B

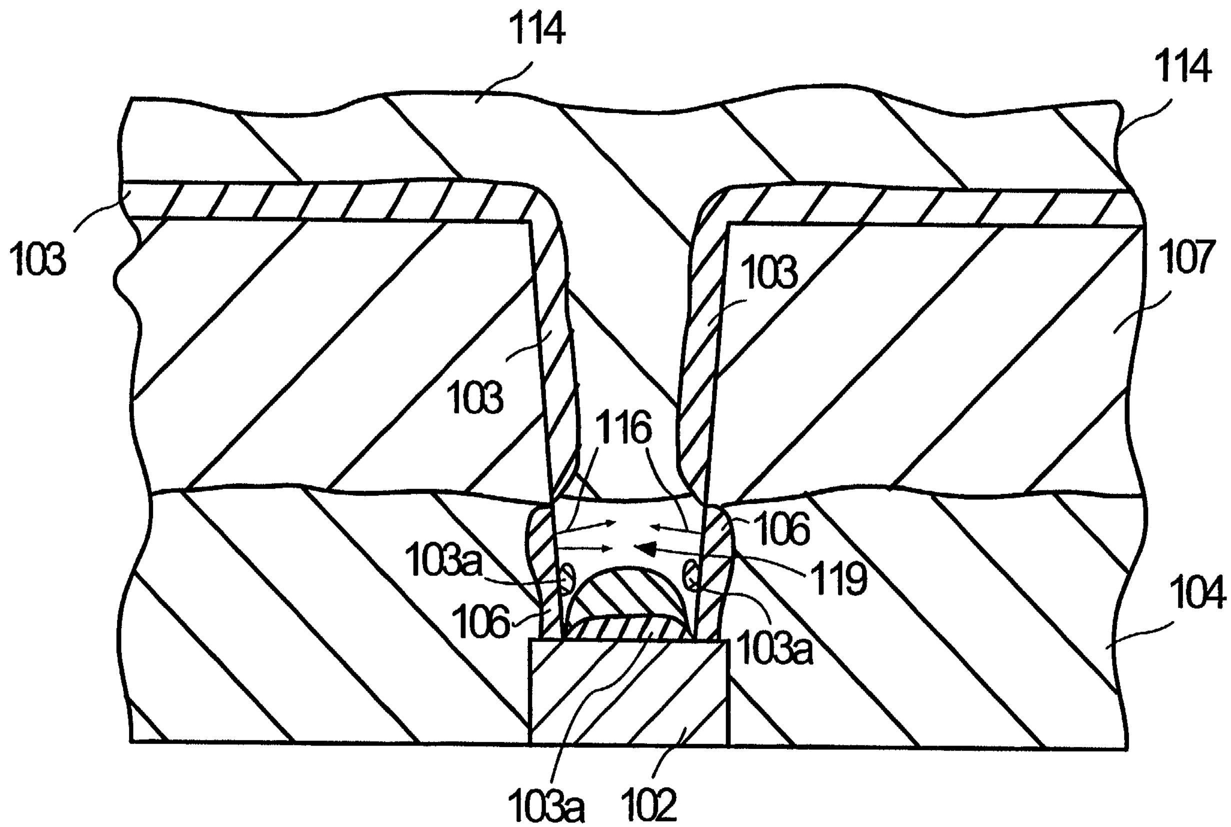

FIG. 1C

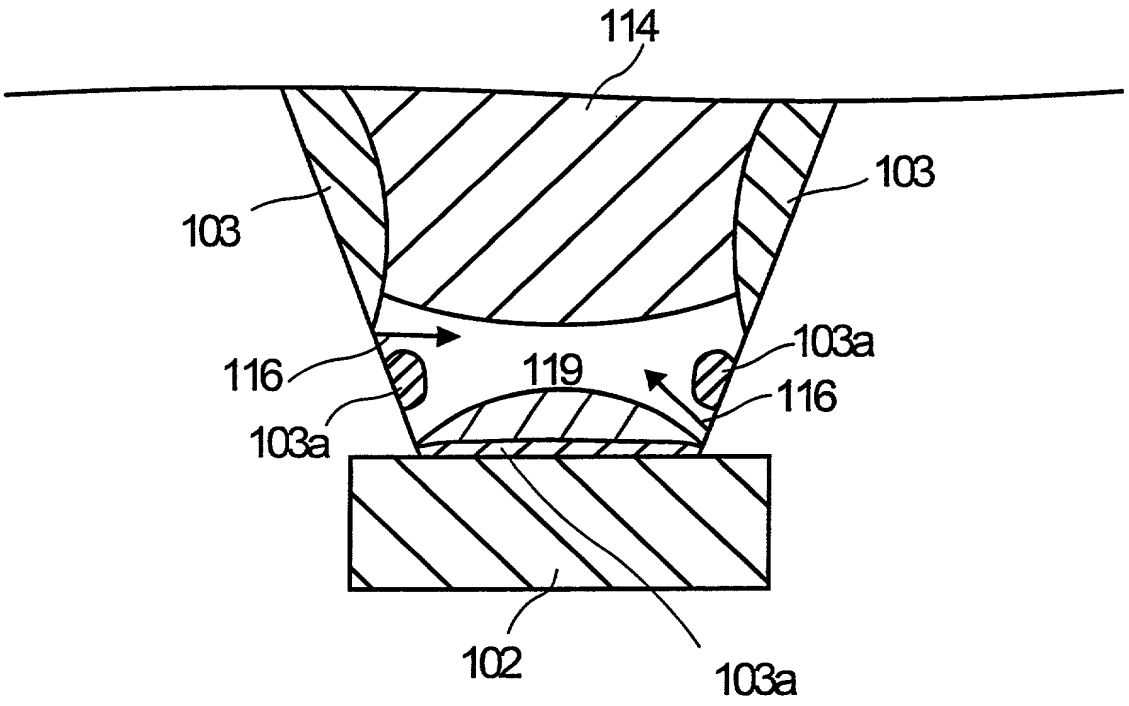

FIG. 1D

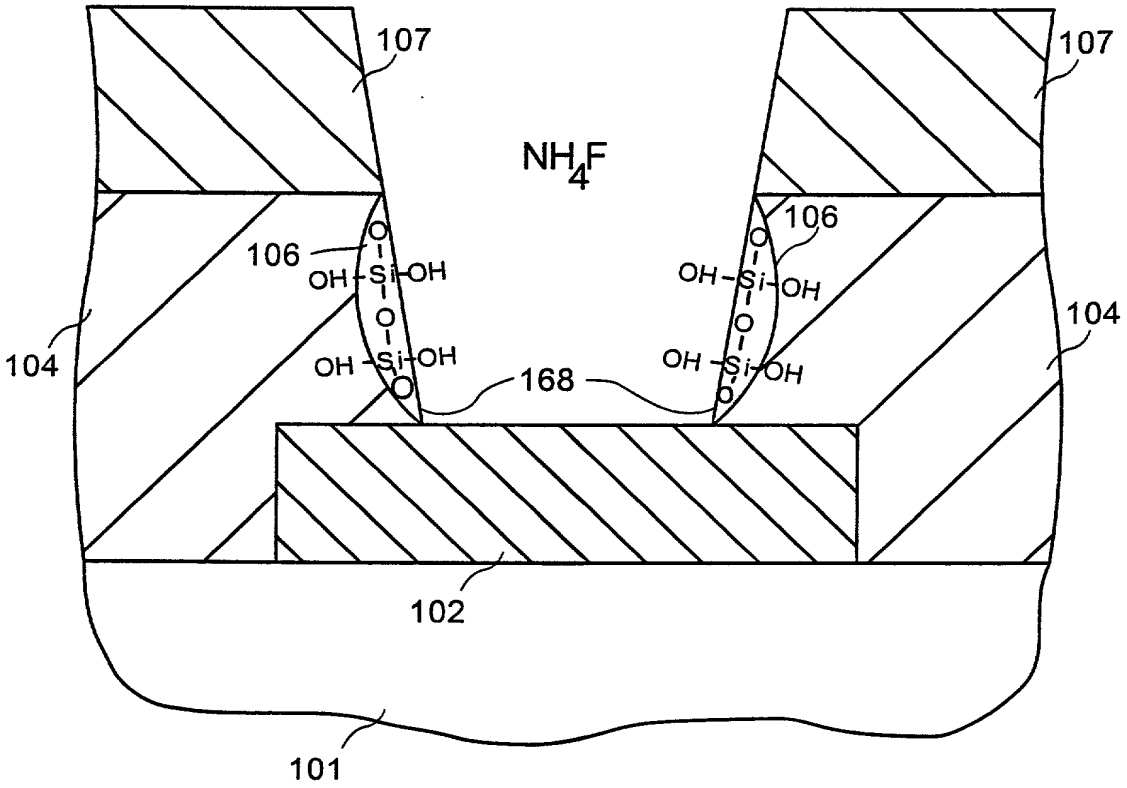
107
107
NH_4F
106
106
OH–Si–OH
OH–Si–OH
OH–Si–OH
OH–Si–OH
104
104
168
102
101

FIG. 2A

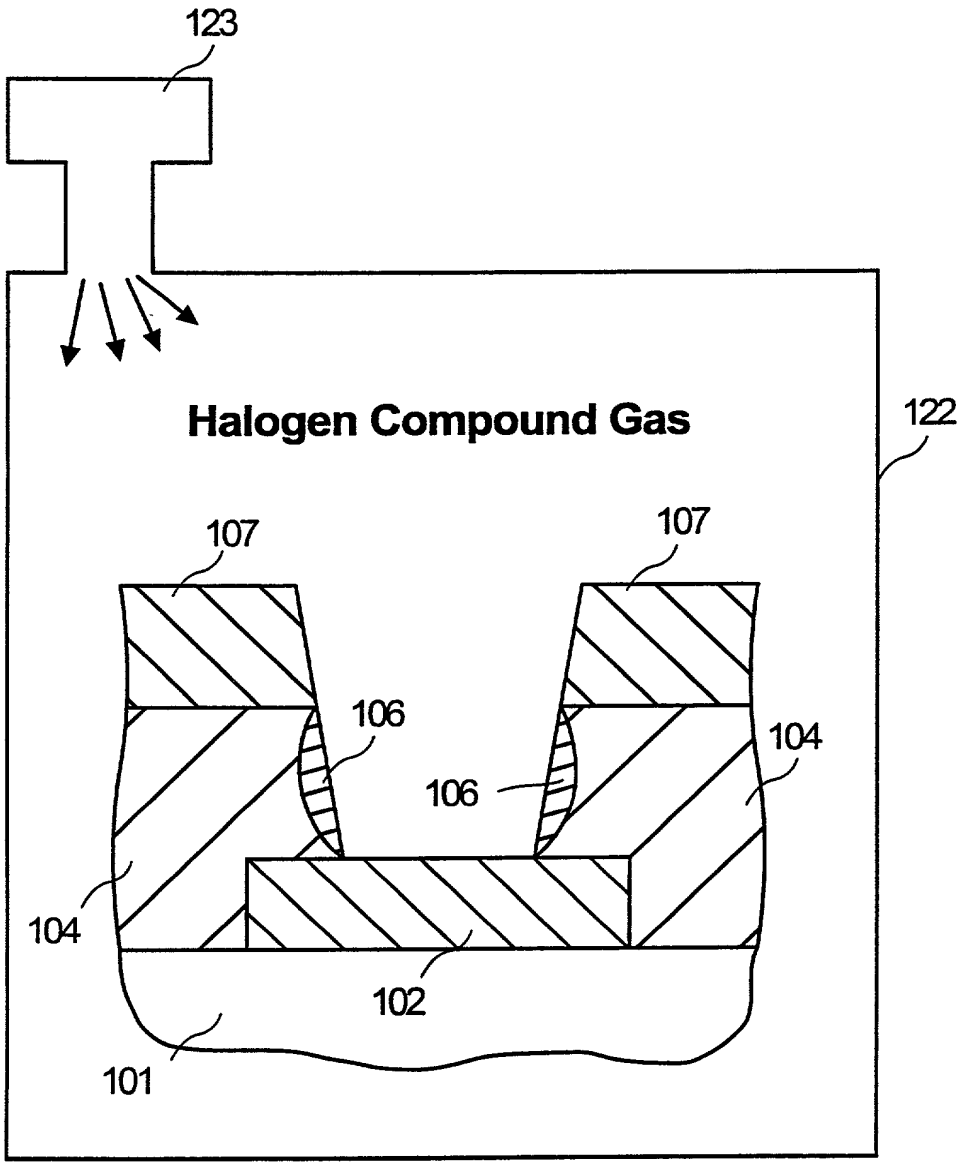

FIG. 2B

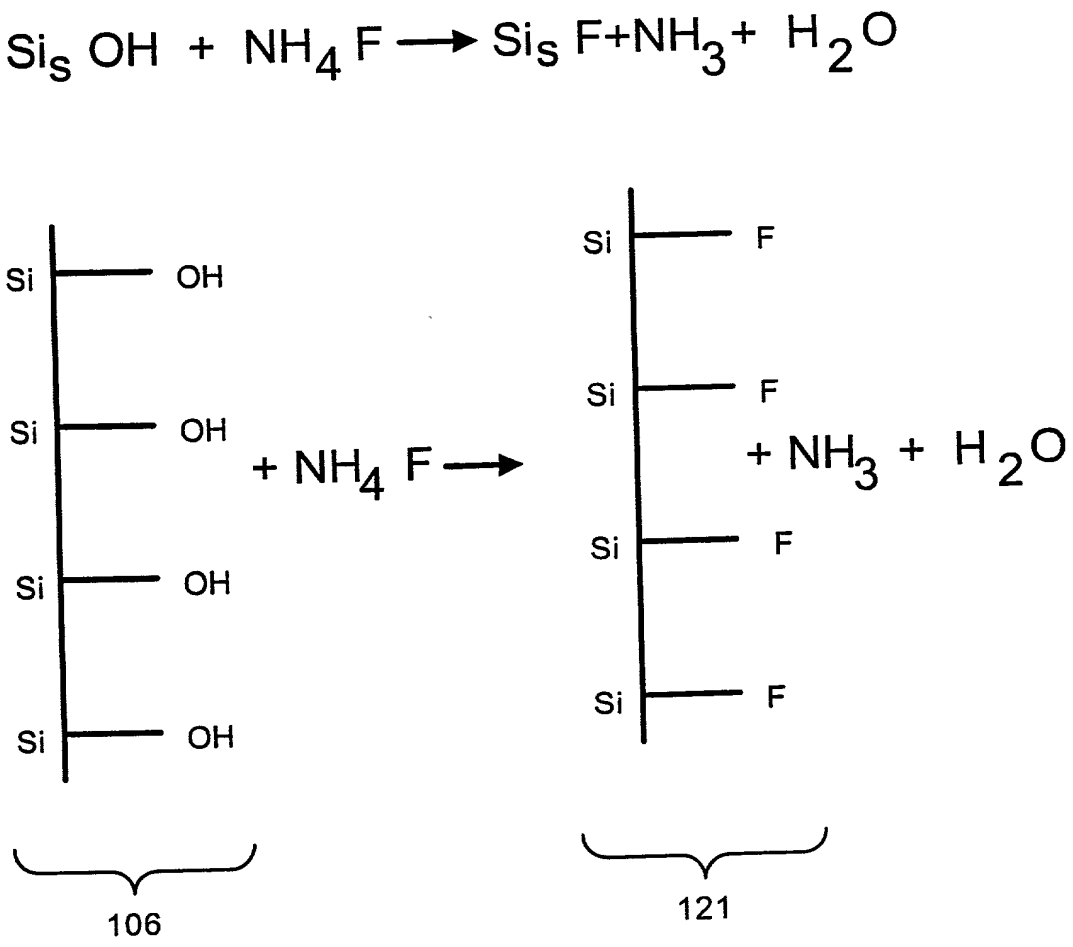
$Si_S\ OH + NH_4F \rightarrow Si_S\ F + NH_3 + H_2O$
Si
OH
Si
OH
Si
OH
Si
OH
+ NH_4F →
Si
F
Si
F
Si
F
Si
F
+ NH_3 + H_2O
106
121

FIG. 2C

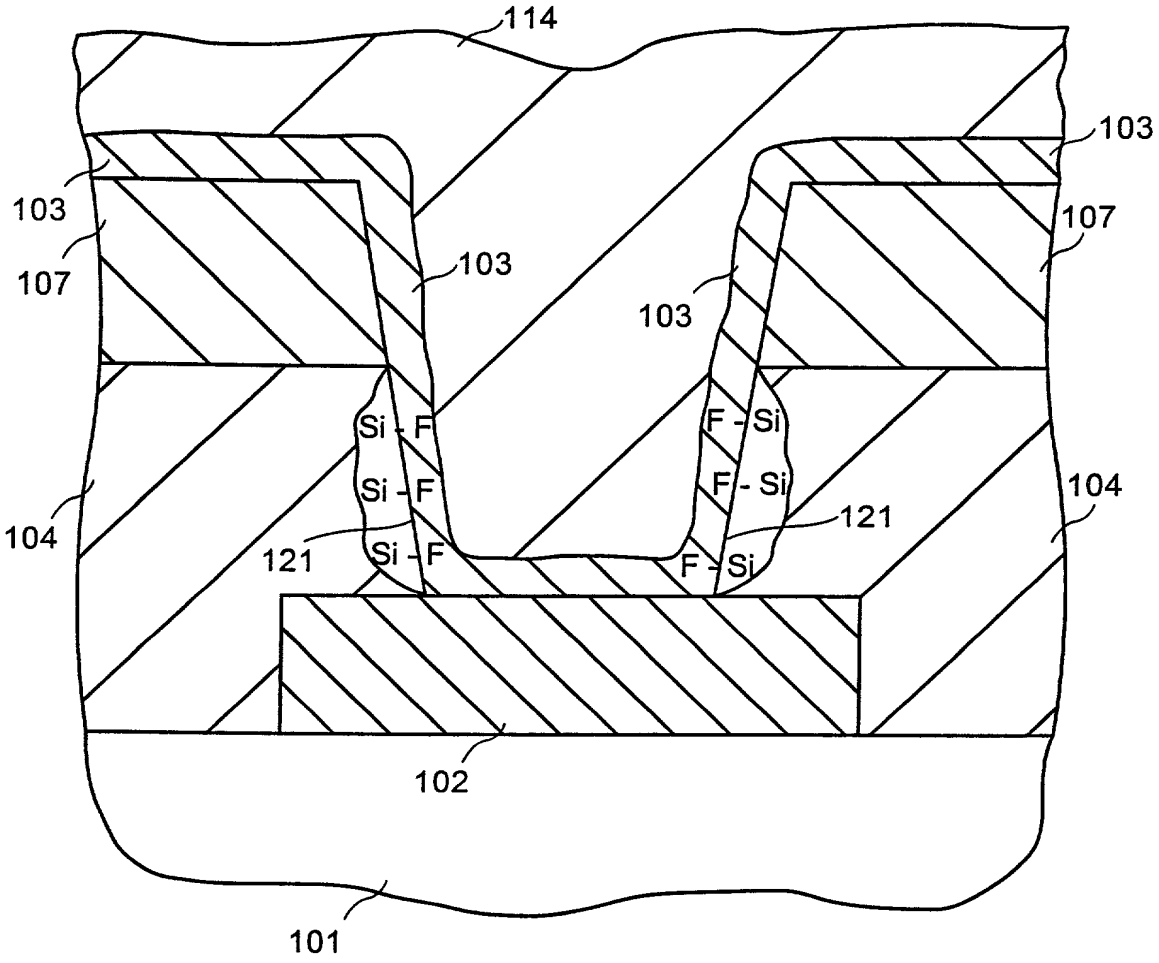
114
103
103
107
103
103
107
Si - F
Si - F
Si - F
F - Si
F - Si
F - Si
104
104
121
121
102
101

FIG. 2D

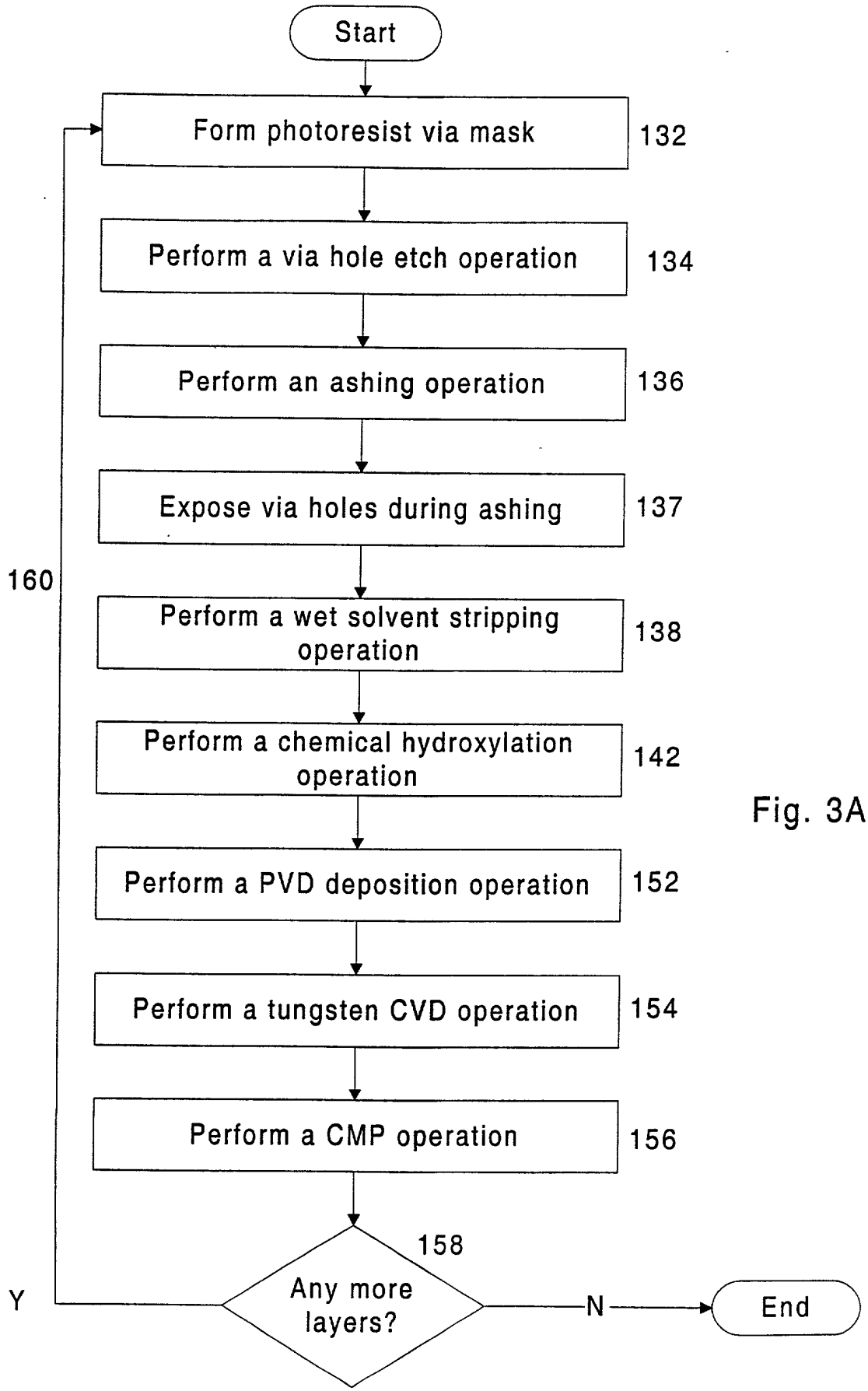
Start
Form photoresist via mask
132
Perform a via hole etch operation
134
Perform an ashing operation
136
Expose via holes during ashing
137
160
Perform a wet solvent stripping operation
138
Perform a chemical hydroxylation operation
142
Perform a PVD deposition operation
152
Perform a tungsten CVD operation
154
Perform a CMP operation
156
158
Any more layers?
Y
N
End

Fig. 3A

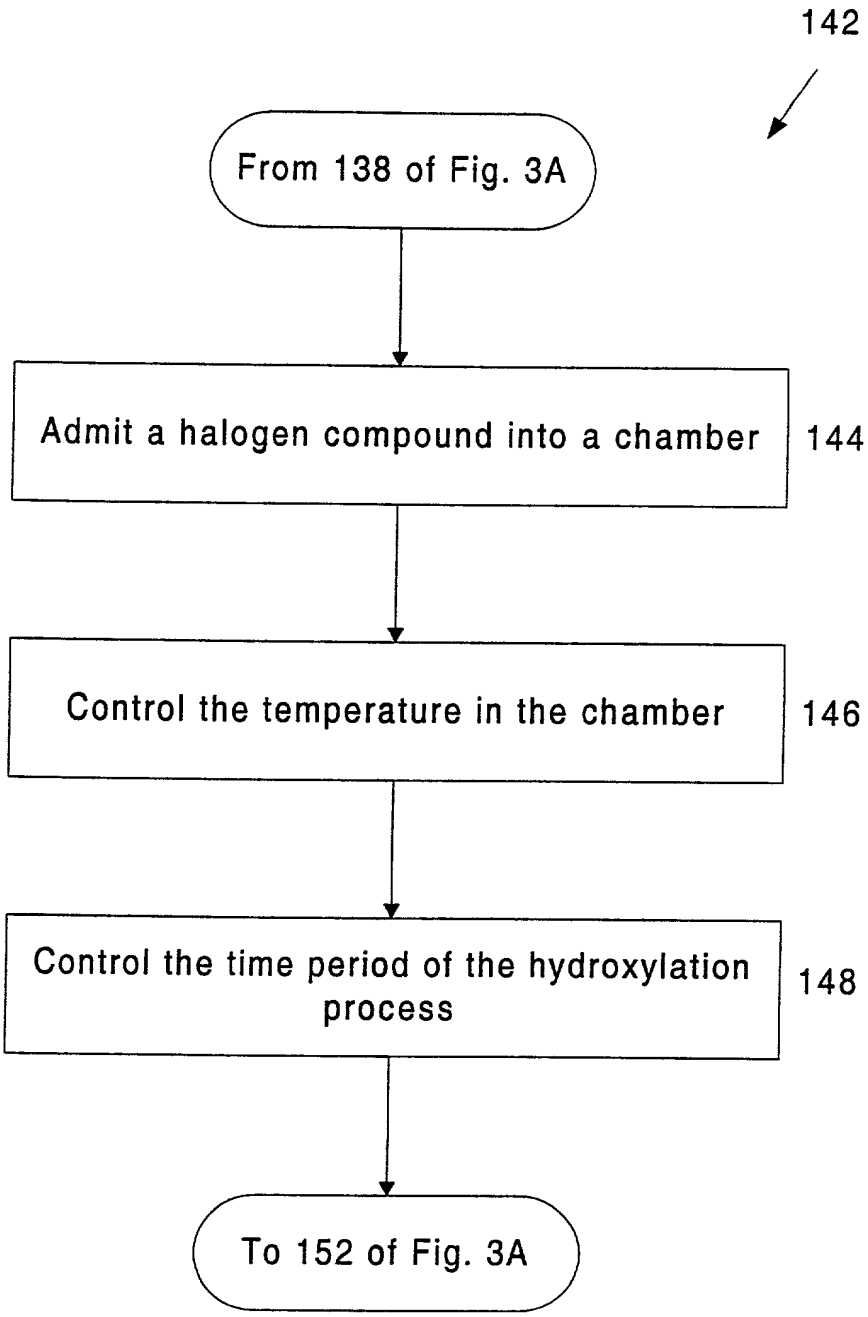
142
From 138 of Fig. 3A
Admit a halogen compound into a chamber
144
Control the temperature in the chamber
146
Control the time period of the hydroxylation process
148
To 152 of Fig. 3A

Fig. 3B

DECLARATION AND POWER OF ATTORNEY FOR ORIGINAL U.S. PATENT APPLICATION

Attorney's Docket No. VT11P204

As a below-named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: RELIABLE VIA STRUCTURES HAVING HYDROPHOBIC INNER WALL SURFACES AND METHODS FOR MAKING THE SAME, the specification of which,

(check one)

1. ☒ is attached hereto.

2. ☐ was filed on _____ as U.S. Application Serial No. _____ and was amended on _____.

3. ☐ was filed on _____ as International PCT Application Serial No. _____ and was amended on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, CFR § 1.56.

I hereby claim foreign priority benefits under Title 35, United States code, § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Benefits Claimed?
_____ (Appl. No.)	_____ (Country)	_____ (Filing Date)	☐ Yes ☐ No
_____ (Appl. No.)	_____ (Country)	_____ (Filing Date)	☐ Yes ☐ No
_____ (Appl. No.)	_____ (Country)	_____ (Filing Date)	☐ Yes ☐ No

I hereby claim the benefit under 35 U.S.C. §119(e) of any United States provisional application(s) listed below:

_____ (Application Serial No.) _____ (Filing Date)

_____ (Application Serial No.) _____ (Filing Date)

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Prior U.S. Application(s)

(Application Serial No.)	(Filing Date)	(Status - patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status - patented, pending, abandoned)

And I hereby appoint the law firm of Martine, Penilla & Kim, LLP, including Peter B. Martine (Reg. No. 32,043); Albert S. Penilla (Reg. No. 39,487); and Raymie H. Kim (Reg. No. 39,462), as my principal attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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830 West Evelyn Avenue
Sunnyvale, California 94086

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Typewritten Full Name of Sole or First Inventor: Rao V. Annapragada — Citizenship: India

Inventor's signature: Rao Annapragada — Date of Signature: 1/14/1999

Residence: (City) San Jose — (State/Country) CA

Post Office Address: 1503 Birchmeadow Court, San Jose, CA 95131

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Docket No: VTI1P304A
R. Annapragada	Group Art Unit: Unassigned
Application No: Unassigned	Examiner: Unassigned
Filed: November 16, 2000	Date: November 16, 2000
For: RELIABLE VIA STRUCTURES HAVING HYDROPHOBIC INNER WALL SURFACES AND METHODS FOR MAKING THE SAME	

CHANGE OF ATTORNEY'S ADDRESS IN APPLICATION

Assistant Commissioner for Patents
Washington, D. C. 20231

Sir:

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